CLAIMS

1. A thin film transistor electronic switching device, comprising:

a source electrode and a drain electrode;

a semiconducting region in contact with and extending between the source and drain electrodes;

a gate electrode disposed for influencing the transconductance of at least part of the semiconducting region; and

an insulating region located between the source and drain electrodes and configured so that the length of the shortest current path through the semiconducting region between the source and drain electrodes is greater than the shortest physical distance between the source and drain electrodes.

2. A device as claimed in claim 1, wherein the insulating region is configured so that the length of the shortest current path through the semiconducting region between the source and drain is greater than 1.05 times the shortest physical distance between the source and drain electrodes.

3. A device as claimed in claim 1 or 2, wherein the shortest current path through the semiconducting region lies closer to the gate electrode than to all paths of the shortest physical distance between the source and drain electrodes .

4. A device as claimed in any preceding claim, wherein the source and drain electrodes comprise an inorganic metallic conductor.

5. A device as claimed in claim 1 to 3, wherein the source and drain electrodes comprise a conducting polymer.

6. A device as claimed in any preceding claim, wherein the semiconducting region comprises a solution processible conjugated polymeric or oligomeric material.

7. A device as claimed in any of claims 1 to 5, wherein the semiconducting region comprises a material of small conjugated molecules with solubilising side chains.

8. A device as claimed in any of claims 1 to 5, wherein the semiconducting region comprises organic-inorganic hybrid materials self-assembled from solution.

9. A device as claimed in any of claims 1 to 5, wherein the semiconducting region comprises an inorganic semiconductor or nanowires.

10. A device as claimed in any preceding claim, wherein the semiconducting region has a mobility exceeding 10^{-3} cm^2/V.

11. A device as claimed in any preceding claim, wherein the semiconductor region is substantially undoped.

12. A device as claimed in any preceding claim, wherein the source and drain electrodes make ohmic contact with the semiconductor region.

13. A device as claimed in any preceding claim, wherein the device has a layer that comprises the source and drain electrodes and a layer that comprises the semiconductor region.

14. A device as claimed in any preceding claim, wherein said insulating region comprises a mesa structure of a dielectric material.

15. A device as claimed in any preceding claim, wherein said insulating region comprises an air gap.

16. A device as claimed in any preceding claim, comprising a gate dielectric layer between the gate electrode and the semiconducting region.

17. A device as claimed in any preceding claim, wherein the shortest physical distance between the source and drain electrodes is less than one micrometre.

18. A method for forming a thin film transistor electronic switching device, the method comprising:

forming a source electrode and a drain electrode;

forming a semiconducting region in contact with and extending between the source and drain electrodes;

forming a gate electrode disposed for influencing the transconductance of at least part of the semiconducting region; and

forming an insulating region located between the source and drain electrodes and configured so that the length of the shortest current path through the semiconducting region between the source and drain electrodes exceeds the shortest physical distance between the source and drain electrodes.

19. A method as claimed in claim 18, wherein the step of forming the semiconducting region is performed after the step of forming the insulating region, the semiconducting region is deposited from solution in contact with the insulating region and the insulating region is capable of repelling the solution from which the semiconducting region is deposited.

20. A method as claimed in claim 19, wherein the insulating region comprises a bulk portion of a first composition and a surface portion of a second composition on to which is deposited the solution from which the semiconducting region is deposited, the surface portion being capable of repelling that solution.

21. A method as claimed in claim 18 to 20, wherein the thickness of the insulating region is in the range from 30 to 80 nm.

22. A method as claimed in any of claims 18 to 21, wherein the source and drain electrodes are formed by inkjet printing.

23. A method as claimed in any of claims 18 to 21, wherein the source and drain electrodes are formed by a continuous film coating technique.

24. A method as claimed in any of claims 18 to 23, wherein one or more components of the device are deposited by vacuum deposition and patterned by photolithography.

25. A method as claimed in any of claims 18 to 23, wherein one or more components of the device are formed by electron beam lithography.

26. A method as claimed in any of claims 18 to 25, wherein said insulating region is defined by a lithographic patterning technique.

27. A method as claimed in any of claims 18 to 25, wherein said insulating region is defined by embossing.

28. A method as claimed in any of claims 18 to 25, wherein said insulating region is formed by depositing an insulating material onto the substrate, wherein the insulating material preferably deposits in the region between the source and drain electrodes, but not on top of the source-drain electrodes.

29. A method as claimed in claim 28, wherein said insulating material is deposited from a liquid phase.

30. A method as claimed in claim 28, wherein said insulating material is deposited from a vapour phase.

31. An electronic switching device substantially as herein described with reference to the accompanying drawings.

32. A method for forming an electronic switching device substantially as herein described with reference to the accompanying drawings.